Amendments to the Specification:

Please replace paragraph on page 4 beginning on line 9 with the following amended paragraph:

In accordance with another feature of the invention, a system analyzer includes a transmitter board for transmitting a copy of signals being produced in a system for analysis by the system analyzer. The copy of such signals comprising serial data, each such data being in a series a low byte serial link and a high byte serial link. The signals include the data and special characters interspersed in a pattern with the data in the low byte serial link and interspersed with the data in such high byte serial link. An analyzer board is adapted for plugging into the transmitter board. The analyzer board includes a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board, and for converting the received data and the special characters interspersed therewith in the low byte serial link into corresponding a low byte parallel link and concurrently converting the received data and the special characters interspersed therewith in the ~~low~~ high byte serial link into a corresponding high byte parallel link. A system is provided for determining whether the data and interspersed pattern of special characters in the converted low byte parallel link mismatch the data and the interspersed pattern of special characters in the converted high byte parallel link, a determined mismatch indicating the high byte parallel link is not aligned with the low byte parallel link, such system maintaining a count of the number of mismatches, such system providing a reset signal to the serializer-deserializer when a predetermined plurality of mismatches has been indicated.

Please replace paragraph on page 4 beginning on line 27 with the following amended paragraph:

In accordance with another feature of the invention, a system analyzer is provided having a transmitter board for transmitting a copy of signals being produced in a system for analysis by the system analyzer, the copy of such signals comprising serial data. Each such data in the series has lower significant bytes thereof in a low byte serial link and has more significant bytes thereof in a high byte serial link. The signals include with the data, special characters interspersed in a pattern with the bytes of each of the data in such low byte serial link and interspersed with the bytes of each of the data in such high byte link serial data. An analyzer board is adapted for plugging into the transmitter board. The analyzer board includes a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board, and for converting the received low significant bytes of each data and the special characters interspersed therewith in the low byte serial link into corresponding lower significant bytes in a parallel low byte link and concurrently converting the received higher significant bytes in each data and the special characters interspersed therewith in the ~~low~~ high byte serial link into corresponding parallel higher significant bytes in a parallel high byte link. A system is provided for determining whether the data and pattern of special characters in the parallel low byte link matches the data and the pattern of special characters in the parallel high byte link, a determined match indicating the high byte parallel link is aligned with the low byte parallel link and a mismatch indicating the high byte parallel link is not aligned with the low byte parallel link, such system maintaining a count of the number of mismatches, such system providing a reset signal when a predetermined plurality of mismatches has been indicated. The reset signal is fed to the serializer-deserializer to reset such serializer-deserializer.